



ISOCOM
COMPONENTS

ICPL332J

DESCRIPTION

The ICPL332J is an advanced 5.0 A output current, easy-to-use, intelligent gate driver which makes IGBT V_{CE} fault protection compact, affordable, and easy-to-implement. Features such as integrated V_{CE} detection, under voltage lockout (UVLO), "soft" IGBT turn-off, isolated open collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

The ICPL332J contains an AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. ICPL332J is ideally suited for driving power IGBTs and MOSFET used in motor control inverter applications. For IGBTs with higher ratings, the ICPL332J can be used to drive a discrete power stage which drives the IGBTs gate.

ICPL332J is supplied in SO16 package.

FEATURES

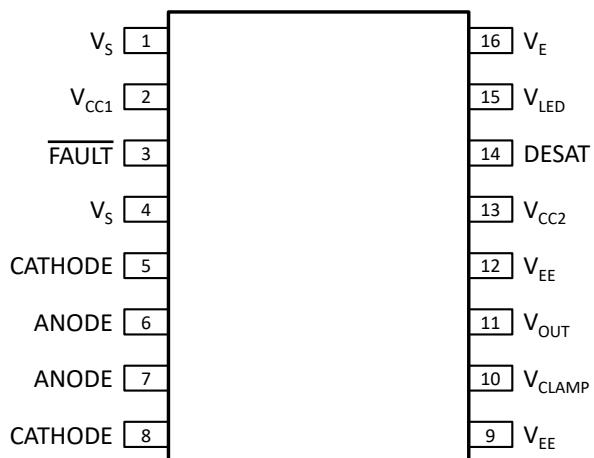
- 5.0A maximum Peak Output Current
- 4.0A minimum Peak Output Current
- Under Voltage Lock Out (UVLO) Protection with Hysteresis
- Desaturation Detection
- 1.7A Miller Clamping
Clamp pin short to V_{EE} if not used
- Open Collector Isolated Fault Feedback
- "Soft" IGBT Turn-Off
- Fault Reset by next LED Turn-On (Low to High) after Fault Mute period
- 200ns maximum Propagation Delay
- 100ns maximum Pulse Width Distortion (PWD)
- 4.5mA maximum Supply Current I_{CC}
- Guaranteed performance over Temperature range -40°C to $+105^{\circ}\text{C}$
- High Common Mode Rejection (CMR)
 $50\text{kV}/\mu\text{s}$ minimum at V_{CM} 1500V
- RoHS Compliant
- UL File E91231

APPLICATIONS

- Isolated IGBT / MOSFET Gate Drive
- Industrial Inverters
- Uninterruptible Power Supply (UPS)
- AC and Brushless DC Motor Drives

ORDER INFORMATION

- Supplied in Tape and Reel



1	V_S	Input Ground
2	V_{CC1}	Positive Input Supply Voltage
3	FAULT	Fault Output
4	V_S	Input Ground
5	CATHODE	Cathode
6	ANODE	Anode
7	ANODE	Anode
8	CATHODE	Cathode
9	V_{EE}	Output Supply Voltage
10	V_{CLAMP}	Miller Clamp
11	V_{OUT}	Gate Drive Voltage Output
12	V_{EE}	Output Supply Voltage
13	V_{CC2}	Positive Output Supply Voltage
14	DESAT	Desaturation Voltage Input
15	V_{LED}	LED Anode
16	V_E	Common Output Supply Voltage (IGBT Emitter)

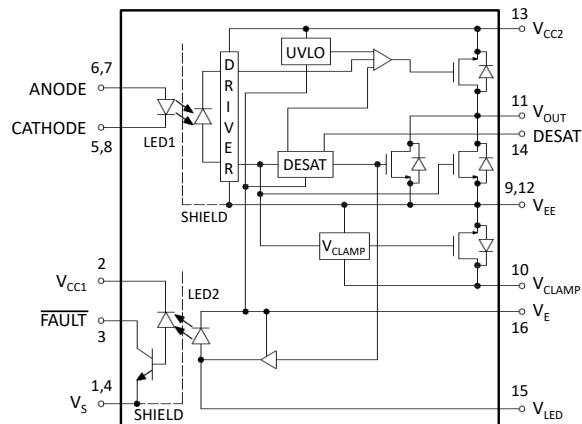
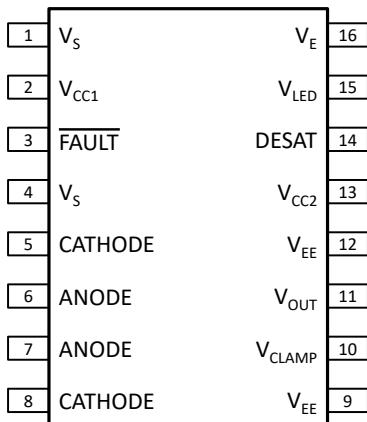
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1	V _S	Input Ground
2	V _{CC1}	Positive Input Supply Voltage (3.3V to 5.5V)
3	FAULT	<p>Fault Output FAULT changes from a high impedance state to a logic low output within 5µs of the voltage on the DESAT pin exceeding an internal reference voltage of 6.7V. FAULT output is an open collector which allows the FAULT outputs from all ICPL332J in a circuit to be connected together in a “wired OR” forming a single fault bus for interfacing directly to the micro-controller.</p>
4	V _S	Input Ground
5	CATHODE	Cathode
6	ANODE	Anode
7	ANODE	Anode
8	CATHODE	Cathode
9	V _{EE}	Output Supply Voltage
10	V _{CLAMP}	Miller Clamp
11	V _{OUT}	Gate Drive Voltage Output
12	V _{EE}	Output Supply Voltage
13	V _{CC2}	Positive Output Supply Voltage
14	DESAT	<p>Desaturation Voltage Input When the voltage on DESAT exceeds an internal reference voltage of 6.7V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state within 5µs.</p>
15	V _{LED}	<p>LED Anode This pin must be left unconnected for guaranteed data sheet performance. (For Optical Coupling Testing only)</p>
16	V _E	Common Output Supply Voltage (IGBT Emitter)

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ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Stresses exceeding the absolute maximum ratings can cause permanent damage to the device.
Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

INPUT LED

Average Input Current	I_F	25mA
Peak Transient Input Current	$I_{F(\text{TRAN})}$	1A
Reverse Input Voltage	V_R	5V
Power Dissipation	P_I	150mW

FAULT

Positive Input Supply Voltage	V_{CC1}	-0.5V to 7V
FAULT Output Current	I_{FAULT}	8mA
FAULT Pin Voltage	V_{FAULT}	-0.5V to V_{CC1}

OUTPUT

"High" Peak Output Current	$I_{OH(\text{PEAK})}$	5A
"Low" Peak Output Current	$I_{OL(\text{PEAK})}$	5A
Total Output Supply Voltage	$V_{CC2} - V_{EE}$	-0.5V to 35V
Positive Output Supply Voltage	$V_{CC2} - V_E$	-0.5V to 35V - ($V_E - V_{EE}$)
Negative Output Supply Voltage	$V_E - V_{EE}$	-0.5V to 15V
Output Voltage	$V_O(\text{PEAK})$	-0.5V to 35V
Peak Clamping Sinking Current	I_{Clamp}	1.7A
Miller Clamping Pin Voltage	V_{Clamp}	-0.5V to V_{CC2}
DESAT Voltage	V_{DESAT}	V_E to $V_E + 10V$
Power Dissipation	P_O	600mW
Junction Temperature	T_J	125°C

TOTAL PACKAGE

Isolation Voltage	V_{ISO}	5000V _{RMS}
Operating Temperature	T_{OP}	-40 to 105°C
Storage Temperature	T_S	-55 to 125°C
Lead Soldering Temperature (10s)		260°C

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Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-40	105	°C
Total Output Supply Voltage	V _{CC2} – V _{EE}	15	30	V
Positive Output Supply Voltage	V _{CC2} – V _E	15 (-0.5)	30 – (V _E –V _{EE})	V
Negative Output Supply Voltage	V _E – V _{EE}	0 (-0.5)	15	V
Input Current (ON)	I _{FL(ON)}	8	12	mA
Input Voltage (OFF)	V _{F(OFF)}	-3.6 (0)	0.8	V

Negative Output Supply Voltage (V_E – V_{EE}) : This supply is optional. Required only when negative gate drive is implemented.



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ELECTRICAL CHARACTERISTICS (Over Recommended Operating Conditions unless Otherwise Specified.
All Typical Values at $V_{CC} - V_{EE} = 30V$, $V_E - V_{EE} = 0V$, $T_A = 25^\circ C$ unless
Otherwise specified.)

INPUT LED

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward Voltage	V_F	$I_F = 10mA$	1.2	1.37	1.8	V
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$	$I_F = 10mA$		-1.237		mV/°C
Reverse Voltage	BV_R	$I_R = 10\mu A$	5			V
Input Threshold Current (Low to High)	I_{FLH}	$I_O = 0A, V_O > 5V$		2.5	6	mA
Input Threshold Voltage (High to Low)	V_{FHL}		0.8	1.26		V
Input Capacitance	C_{IN}	$f = 1MHz, V_F = 0V$		33		pF

FAULT

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Logic Low Output Voltage	V_{FAULT}	$I_{FAULT} = 1.1mA, V_{CC1} = 5.5V$			0.4	V
		$I_{FAULT} = 1.1mA, V_{CC1} = 3.3V$			0.4	
Logic High Output Current	I_{FAULT}	$V_{FAULT} = 5.5V, V_{CC1} = 5.5V$			0.5	μA
		$V_{FAULT} = 3.3V, V_{CC1} = 3.3V$			0.3	



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Otherwise specified.)

OUTPUT

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
High Level Supply Current	I_{CC2H}	$I_F = 7$ to $16mA$ Output Open		2.4	4.5	mA
Low Level Supply Current	I_{CC2L}	$V_F = 0$ to $0.8V$ Output Open		2.5	4.5	mA
High Level Output Current	I_{OH}	$V_O = V_{CC2} - 3V$ Pulse Width $50\mu s$ max			-2.0	A
		$V_O = V_{CC2} - 7V$ Pulse Width $10\mu s$ max (Note 1)			-5.0	A
Low Level Output Current	I_{OL}	$V_O = V_{EE} + 2V$ Pulse Width $50\mu s$ max	2.0	1.5		A
		$V_O = V_{EE} + 6V$ Pulse Width $10\mu s$ max (Note 1)	5.0			A
High Level Output Voltage	V_{OH}	$I_O = -100mA$, $I_F = 10mA$ (Notes 2, 3, 4)	$V_{CC} - 1.2$	$V_{CC} - 1.0$		V
Low Level Output Voltage	V_{OL}	$I_O = 100mA$, $I_F = 0mA$		$V_{EE} + 0.1$	$V_{EE} + 0.25$	V
Clamp Low Level Sinking Current	I_{CL}	$V_O = V_{EE} + 2.5V$	0.5	4.0		A
Blanking Capacitor Charging Current	I_{CHG}	$V_{DESAT} = 2V$	-0.13	-0.24	-0.33	mA
Blanking Capacitor Discharge Current	I_{DSCHG}	$V_{DESAT} = 7V$	10	30		mA
DESAT Threshold	V_{DESAT}	$V_{CC2} - V_E > V_{UVLO-}$	6	6.5	7.5	V
Clamp Pin Threshold Voltage	V_{tClamp}			2.0		V
UVLO Threshold	V_{UVLO+}	$V_O > 5V$, $I_F = 10mA$	10.5	11.6	12.5	V
	V_{UVLO-}	$V_O < 5V$, $I_F = 10mA$	9.2	10.3	11.1	
UVLO Hysteresis	$UVLO_{HYS}$	$V_{UVLO+} - V_{UVLO-}$		1.3		V



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Otherwise specified.)

SWITCHING

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Propagation Delay Time to High Output Level	t_{PLH}	$R_g = 10\Omega$, $C_g = 10nF$, $f = 10kHz$, Duty Cycle = 50% $I_F = 10mA$ $V_{CC2} = 30V$	50		200	ns
Propagation Delay Time to Low Output Level	t_{PHL}		50		200	
Pulse Width Distortion $ t_{PHL} - t_{PLH} $ for any given Device	PWD		-80		80	
Propagation Delay Difference $(t_{PHL} - t_{PLH})$ between any two Devices under same test conditions	PDD		-100		100	
Output Rise Time (10% to 90%)	t_r			50		
Output Fall time (90% to 10%)	t_f			50		
DESAT Sense to 90% V_O Delay	$t_{DESAT(90\%)}$	$C_{DESAT} = 100pF$ $R_g = 10\Omega$ $C_g = 10nF$		0.25	0.5	μs
DESAT Sense to 10% V_O Delay	$t_{DESAT(10\%)}$			2	3	
DESAT Sense to Low Level \overline{FAULT} Signal Delay	$t_{DESAT(\overline{FAULT})}$	$C_{DESAT} = 100pF$ $R_F = 2.1k\Omega$, $C_F = 1nF$ $R_g = 10\Omega$, $C_g = 10nF$		0.25	0.5	
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(Low)}$	$C_{DESAT} = 100pF$ $R_F = 2.1k\Omega$ $R_g = 10\Omega$, $C_g = 10nF$		0.25		
DESAT input Mute	$t_{DESAT(MUTE)}$		5			
RESET to High Level \overline{FAULT} Signal Delay	$t_{(RESET(\overline{FAULT}))}$	$C_{DESAT} = 100pF$ $R_F = 2.1k\Omega$ $R_g = 10\Omega$, $C_g = 10nF$	0.2	1	2	



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Otherwise specified.)

SWITCHING

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Common Mode Transient Immunity at High Level Output	CM _H	$I_F = 10mA$ $R_F = 2.1k\Omega$, $C_F = 15pF$ $V_{CM} = 1500V$ $V_{CC2} = 30V$ $T_A = 25^\circ C$ Split Resistors Network with Ratio 1:1 at Input LED1	15			kV/μs
		$I_F = 10mA$ $R_F = 2.1k\Omega$, $C_F = 1nF$ $V_{CM} = 1500V$ $V_{CC2} = 30V$ $T_A = 25^\circ C$ Split Resistors Network with Ratio 1:1 at Input LED1	50			
Common Mode Transient Immunity at Low Level Output	CM _L	$V_F = 0V$ $R_F = 2.1k\Omega$, $C_F = 15pF$ $V_{CM} = 1500V$ $V_{CC2} = 30V$	15			
		$V_F = 0V$ $R_F = 2.1k\Omega$, $C_F = 1nF$ $V_{CM} = 1500V$ $V_{CC2} = 30V$	50			

ISOLATION

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
Isolation Voltage	V_{ISO}	$R.H. \leq 40\% - 60\%$ $T_A = 25^\circ C$ $t = 1 min$	5000			V
Input - Output Resistance	R_{I-O}	$V_{I-O} = 500VDC$		10^9		Ω
Input - Output Capacitance	C_{I-O}	$f = 1MHz$, $T_A = 25^\circ C$		1.3		pF

Device is considered a two terminal device : pins 1 to 8 are shorted together and pins 9 to 16 are shorted together



ICPL332J

Notes :

1. Output Current at Maximum Pulse Width 10us : This value is intended to allow for component tolerances for designs with I_O peak minimum 4.0A. Derate linearly from 5.0A to 2.5A at +105°C. This compensates for increased I_O PEAK due to changes in V_{OL} over temperature.
2. 15V is the recommended minimum operating positive supply voltage ($V_{CC2} - V_E$) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5V. For High Level Output Voltage testing, V_{OH} is measured with a DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
3. Maximum Pulse Width 1.0ms.
4. To clamp the output voltage at $V_{CC} - 1$ V, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 100mA while the output is high.
5. Once V_O of the ICPL332J is allowed to go high ($V_{CC2} - V_E > V_{UVLO+}$), the DESAT detection feature of the ICPL332J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} is increased from 0V to above V_{UVLO+} , DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-} . Thus, the DESAT detection and UVLO features of the ICPL332J work in conjunction to ensure constant IGBT protection.
6. V_{UVLO+} : This is the "Increasing" (i.e. turn-on or "Positive going" direction) of $V_{CC2} - V_E$.
7. V_{UVLO-} : This is the "Decreasing" (i.e. turn-off or "Negative going" direction) of $V_{CC2} - V_E$.
8. Switching Time Test Load condition approximates the gate load of a 1200 V/150A IGBT.
9. PWD and PDD measured from ANODE, CATHODE of LED to V_{OUT} .
10. DESAT Sense to Low Level FAULT Signal Delay : This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
11. DESAT Sense to DESAT Low Propagation Delay : This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
12. Auto Reset: This is the amount of time (DESAT Input Mute) when V_{OUT} will be asserted low after DESAT threshold is exceeded.
13. Common Mode Transient Immunity in High state is the maximum tolerable negative dV_{CM}/dt on the trailing edge of the common mode impulse signal, V_{CM} , to assure that the output will remain in High state ($V_O > 15V$ or FAULT > 2V). Split resistors network with a ratio of 1:1 is needed at input LED1.
14. Common Mode Transient Immunity in Low state is the maximum tolerable positive dV_{CM}/dt on the leading edge of the common mode impulse signal, V_{CM} , to assure that the output will remain Low state ($V_O < 1V$ or FAULT < 0.8V).



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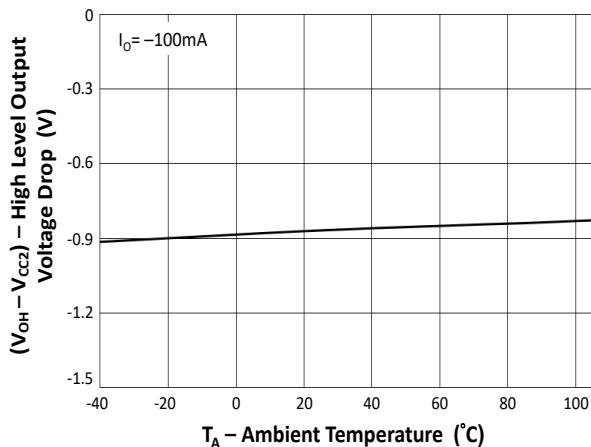


Fig 1 High Level Output Voltage Drop vs
Ambient Temperature

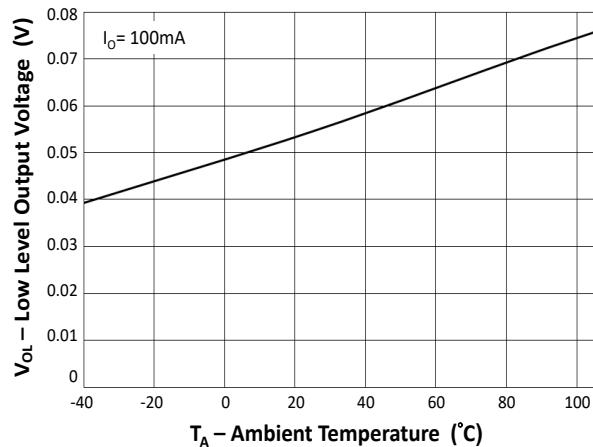


Fig 2 Low Level Output Voltage vs
Ambient Temperature

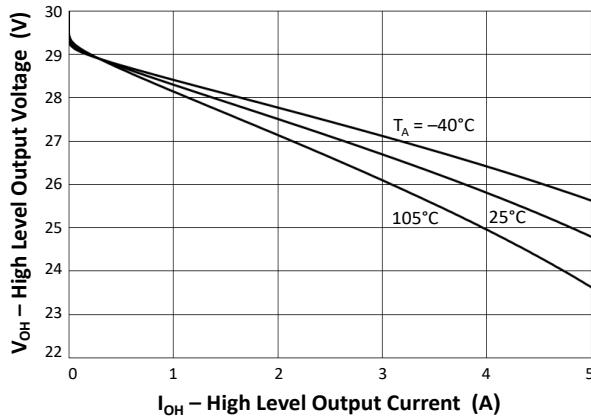


Fig 3 High Level Output Voltage vs
High Level Output Current

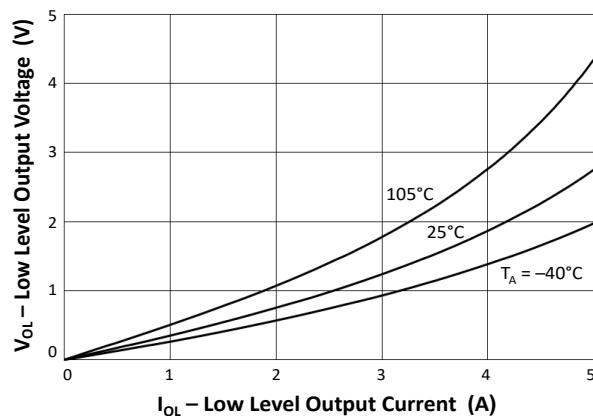


Fig 4 Low Level Output Voltage vs
Low Level Output Current

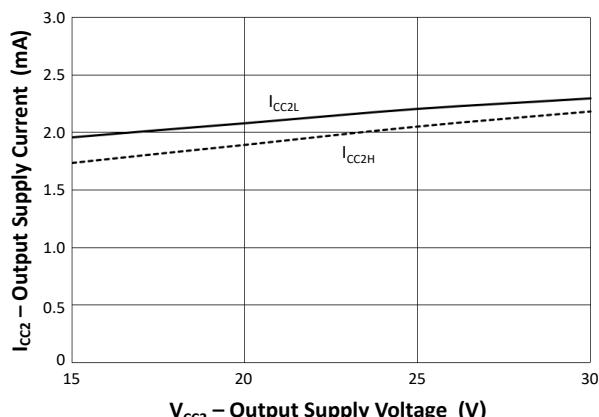


Fig 5 I_{CC2} Output Supply Current vs
 V_{CC2} Output Supply Voltage

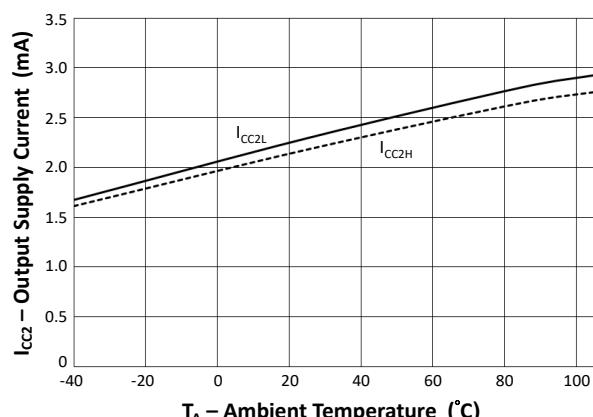


Fig 6 I_{CC2} Output Supply Current vs
Ambient Temperature



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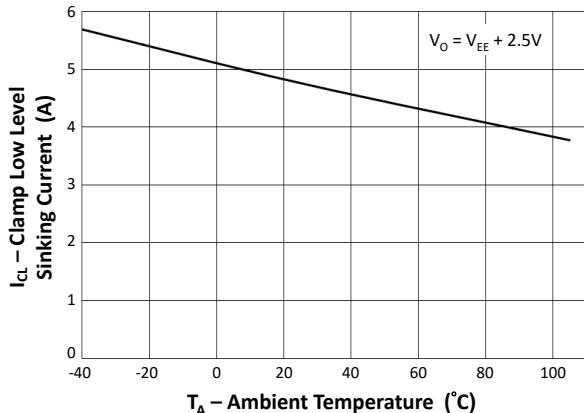


Fig 7 Clamp Low Level Sinking Current vs Ambient Temperature

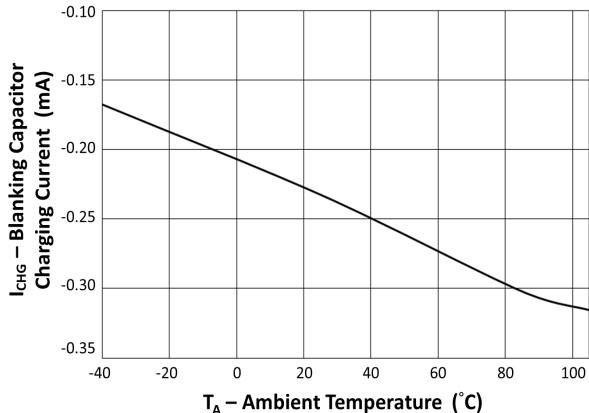


Fig 8 Blanking Capacitor Charging Current vs Ambient Temperature

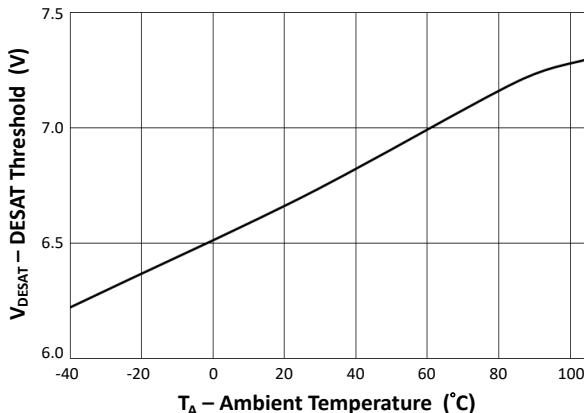


Fig 9 DESAT Threshold Voltage vs Ambient Temperature

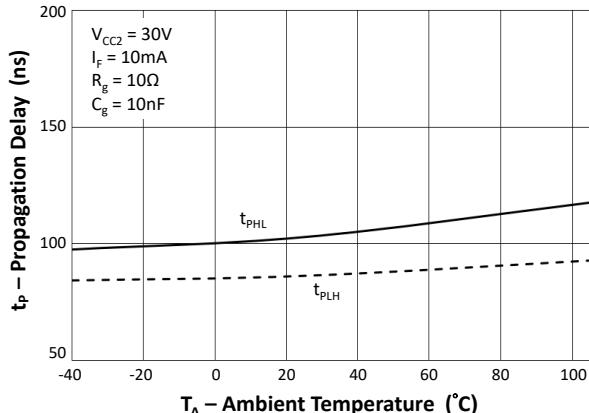


Fig 10 Propagation Delay vs Ambient Temperature

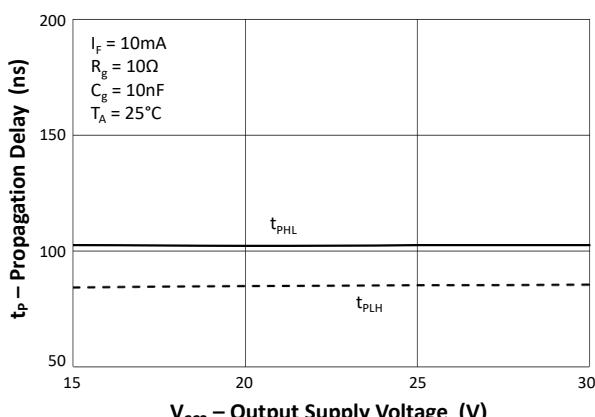


Fig 11 Propagation Delay vs Output Supply Voltage

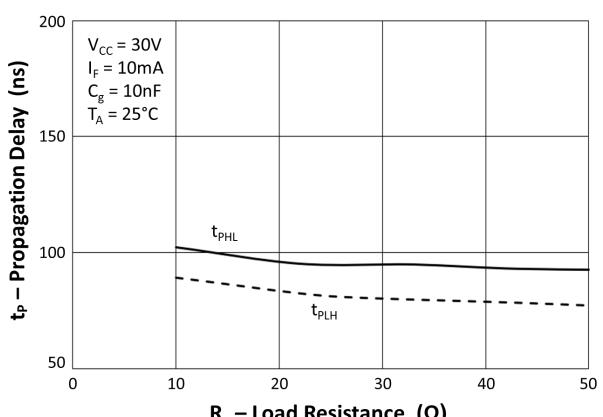


Fig 12 Propagation Delay vs Load Resistance



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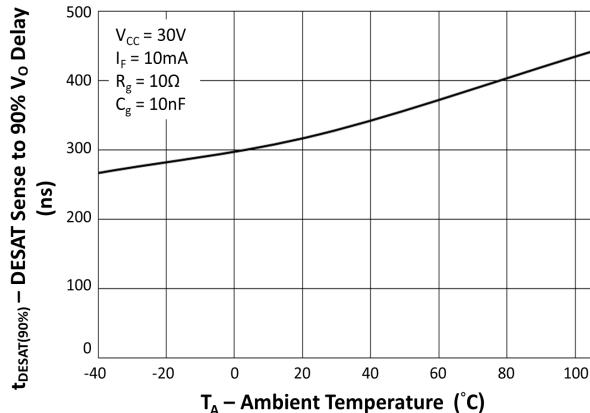


Fig 13 DESAT Sense to 90% Output Voltage Delay vs Ambient Temperature

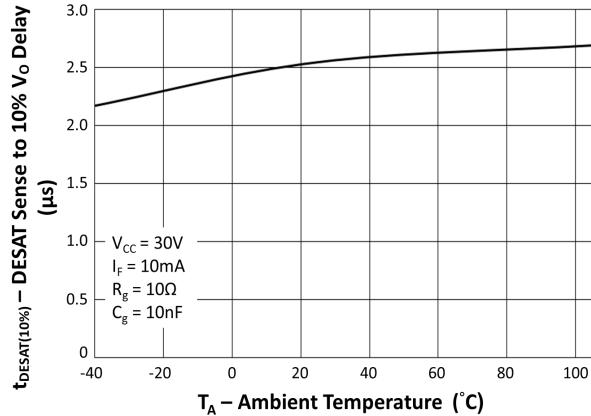


Fig 14 DESAT Sense to 10% Output Voltage Delay vs Ambient Temperature

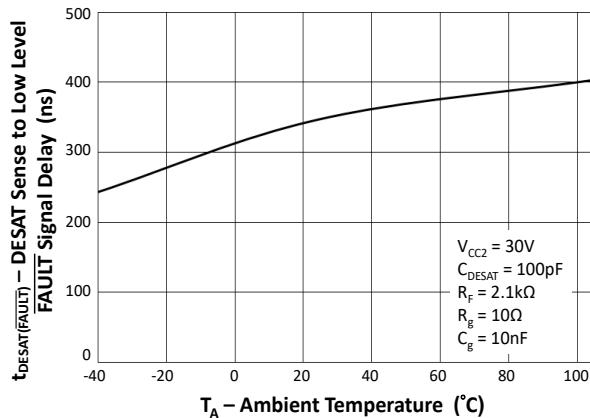


Fig 15 DESAT Sense to Low Level FAULT Signal Delay vs Ambient Temperature

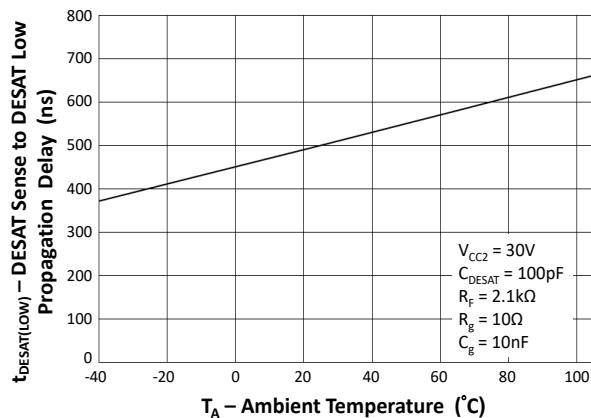


Fig 16 DESAT Sense to DESAT Low vs Ambient Temperature

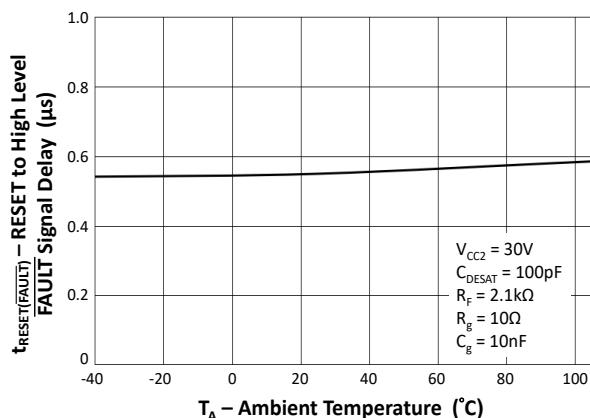


Fig 17 RESET to High Level FAULT Signal Delay vs Ambient Temperature



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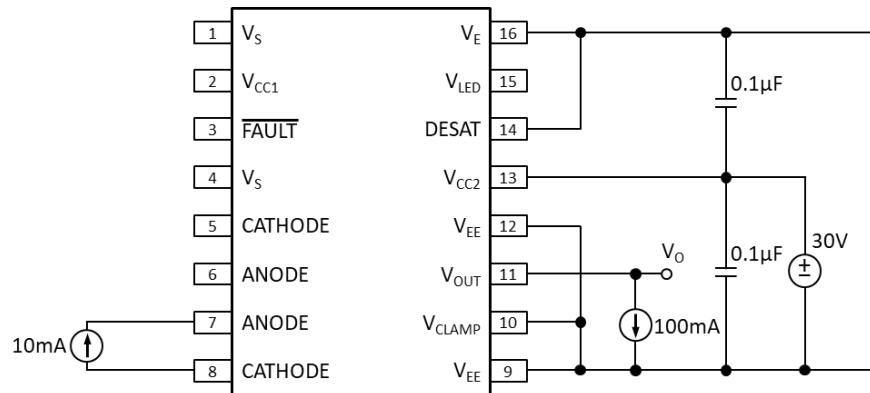


Fig 18 V_{OH} Test Circuit

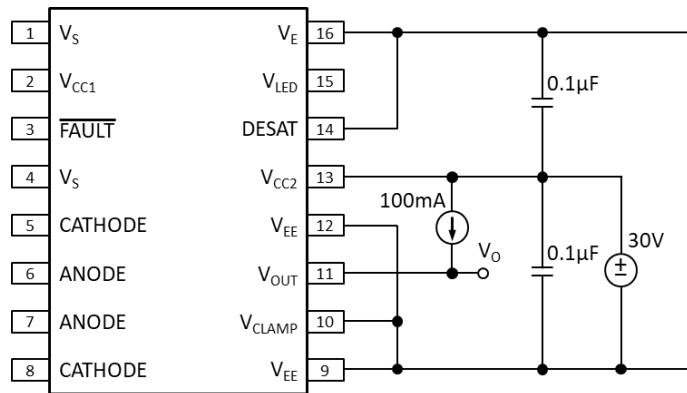


Fig 19 V_{OL} Test Circuit

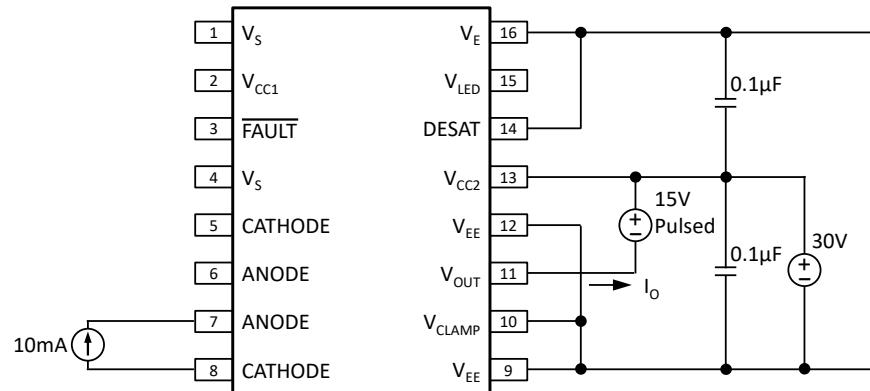


Fig 20 I_{OH} Test Circuit



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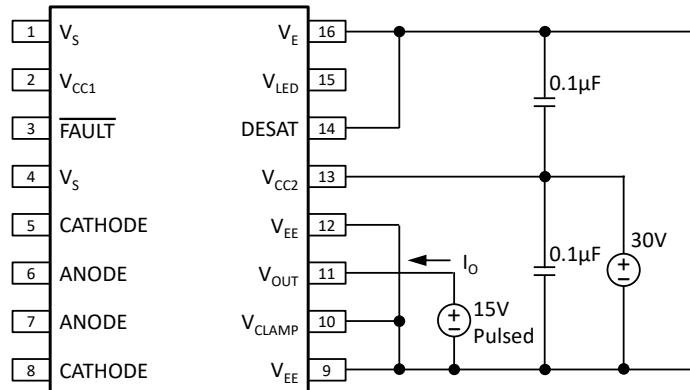


Fig 21 I_{OL} Test Circuit

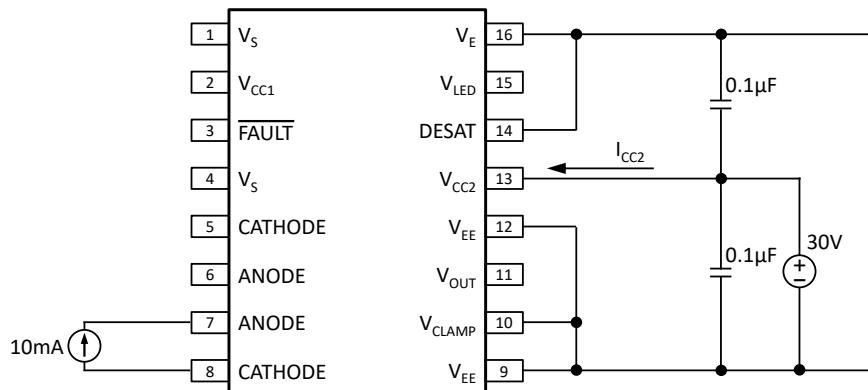


Fig 22 I_{CC2H} Test Circuit

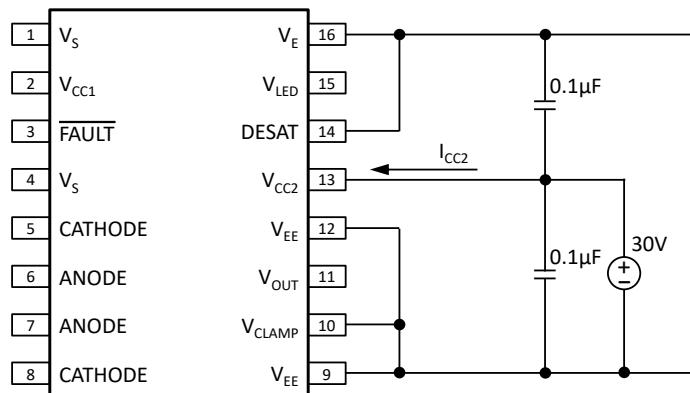


Fig 23 I_{CC2L} Test Circuit



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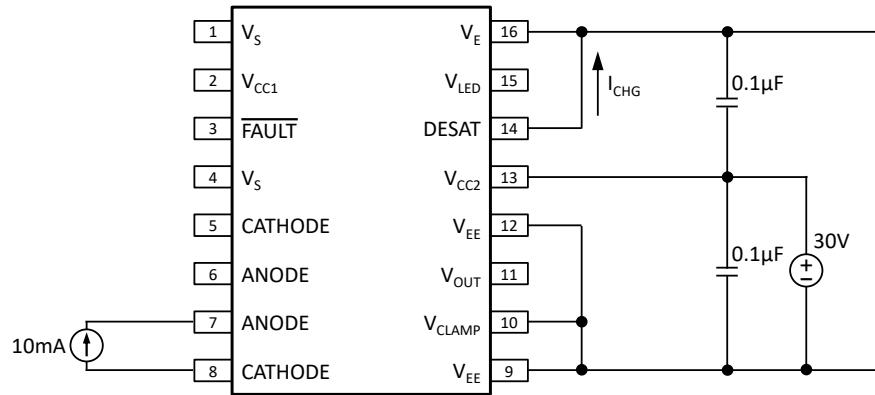


Fig 24 I_{CHG} Test Circuit

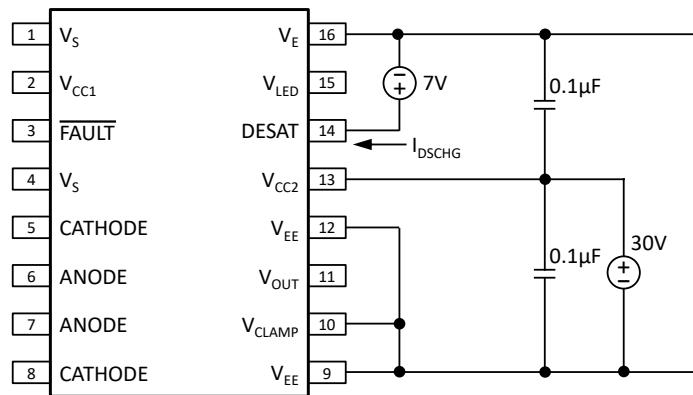


Fig 25 I_{DSCHG} Test Circuit



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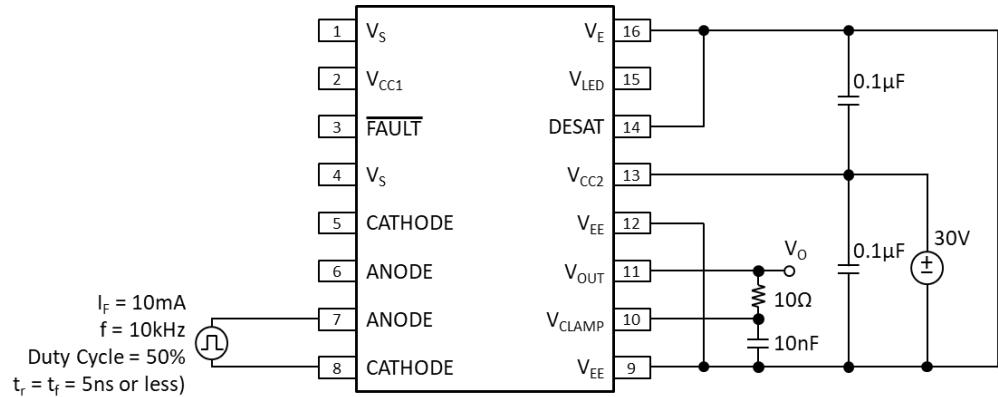
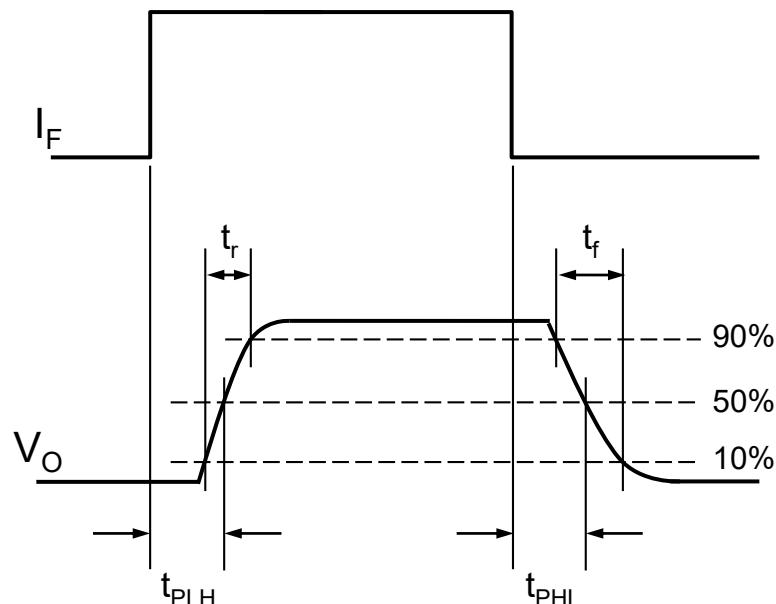


Fig 26 Propagation Delay (t_{PLH} and t_{PHL}), Rise Time (t_r) and Fall Time (t_f) Test Circuit



Propagation Delay (t_{PLH} and t_{PHL}), Rise Time (t_r) and Fall Time (t_f) Timing Waveforms



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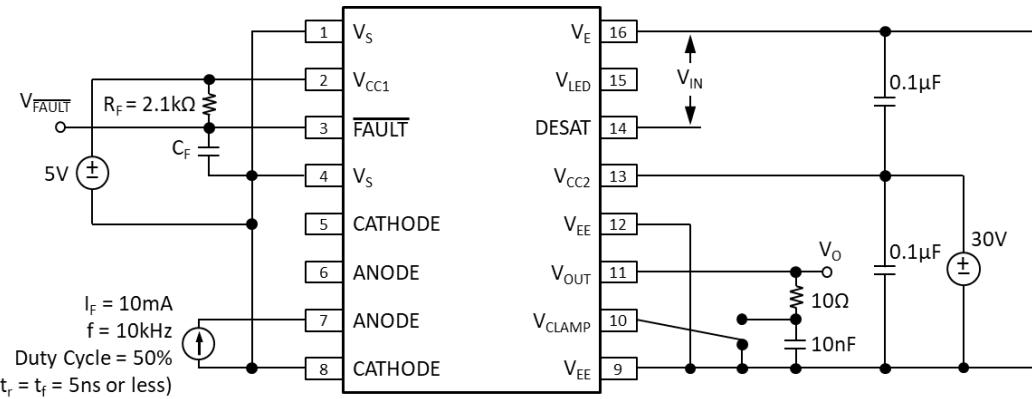
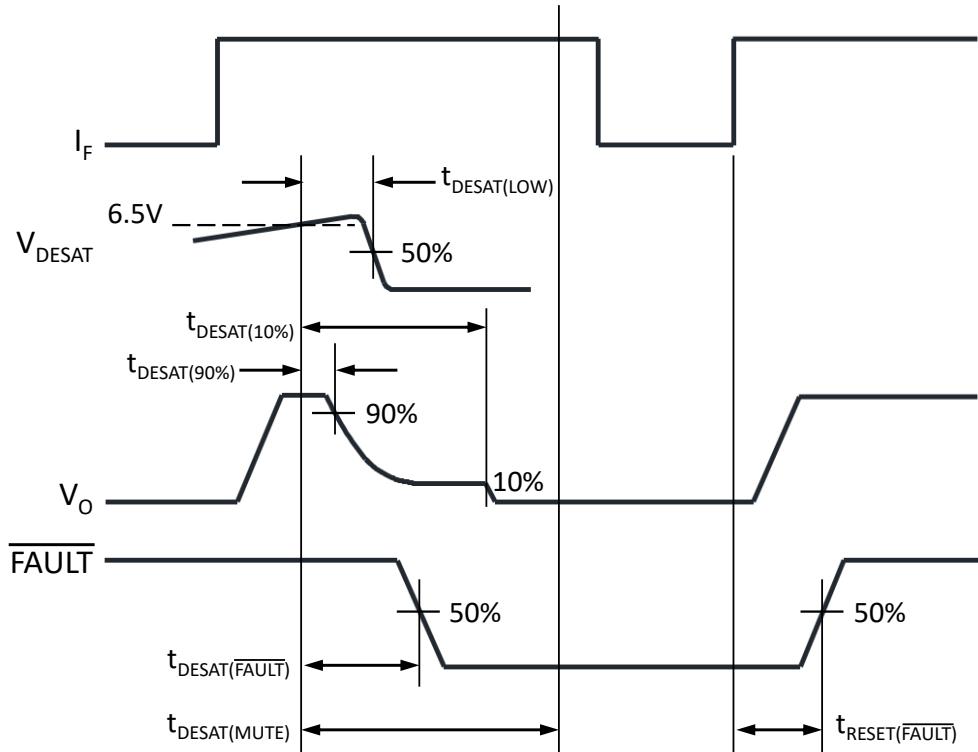


Fig 27 t_{DESAT} Fault Test Circuit



DESAT \overline{FAULT} Timing Waveforms



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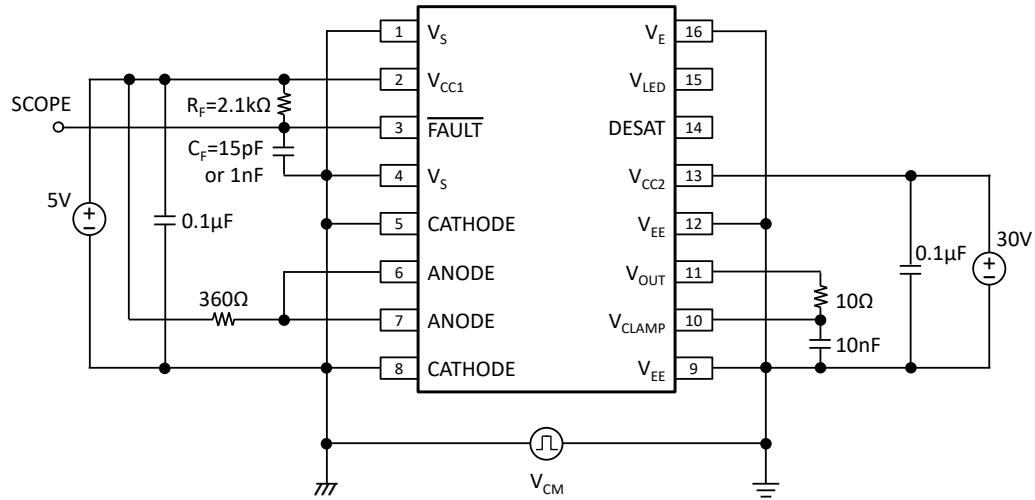


Fig 28 Common Mode Transient Immunity Test Circuit LED2 ON

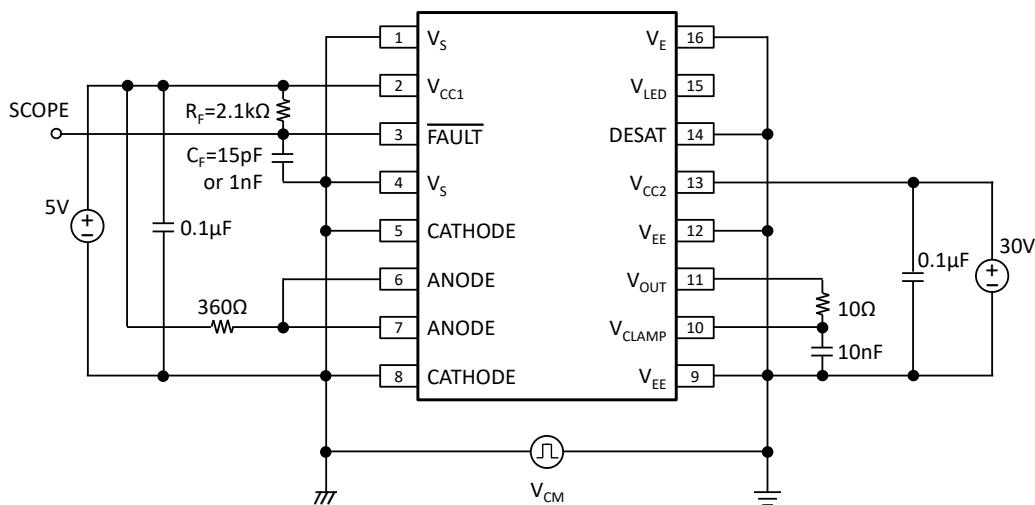


Fig 29 Common Mode Transient Immunity Test Circuit LED2 OFF



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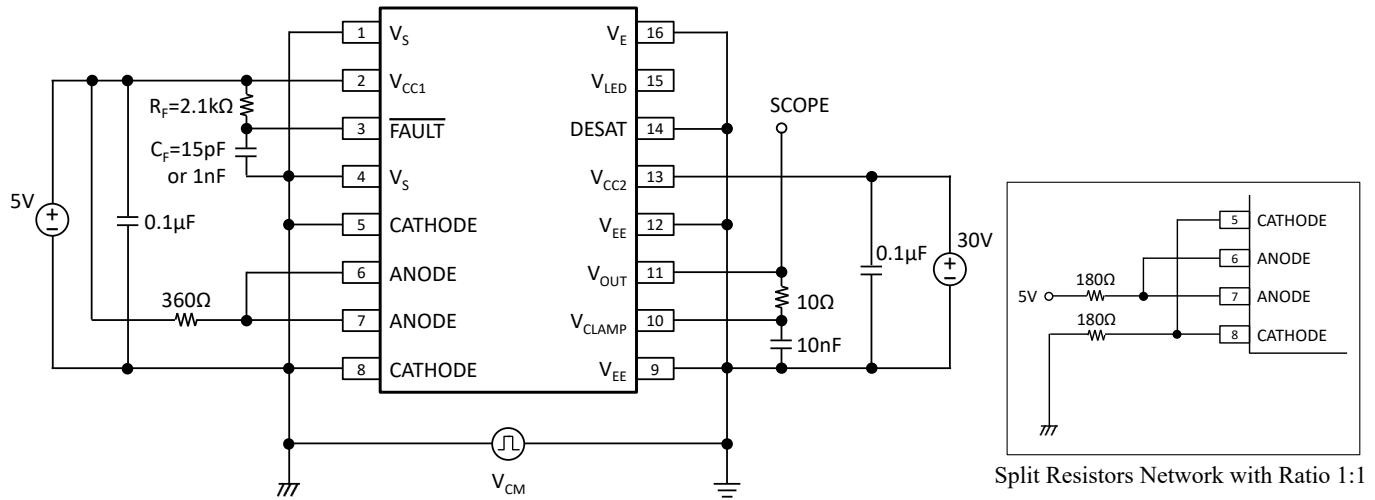


Fig 30 Common Mode Transient Immunity Test Circuit LED1 ON

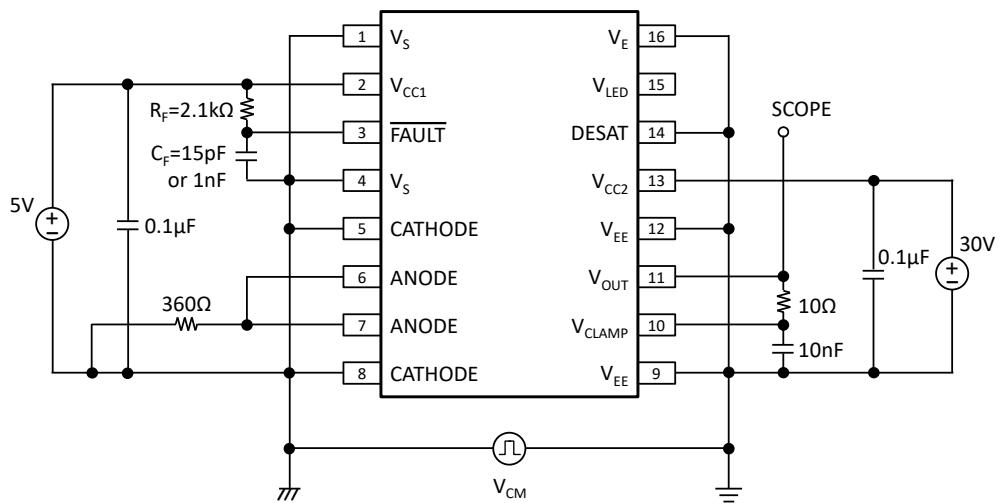


Fig 31 Common Mode Transient Immunity Test Circuit LED1 OFF



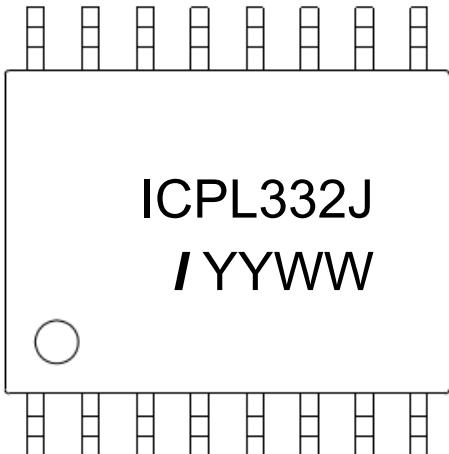
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ORDER INFORMATION

ICPL332J			
After PN	PN	Description	Packing quantity
None	ICPL332J	Surface Mount Tape & Reel	850 pcs per reel

DEVICE MARKING



ICPL332J Device Part Number

I Isocom

YY 2 digit Year Code

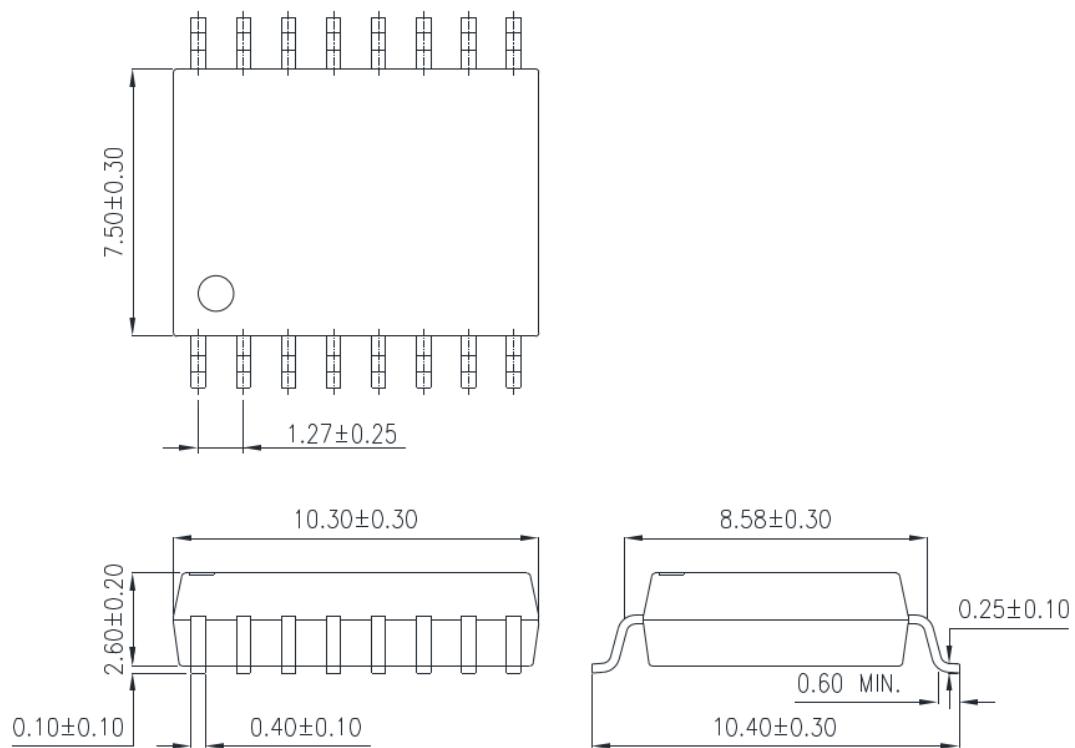
WW 2 digit Week Code



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PACKAGE DIMENSIONS in mm (inch)

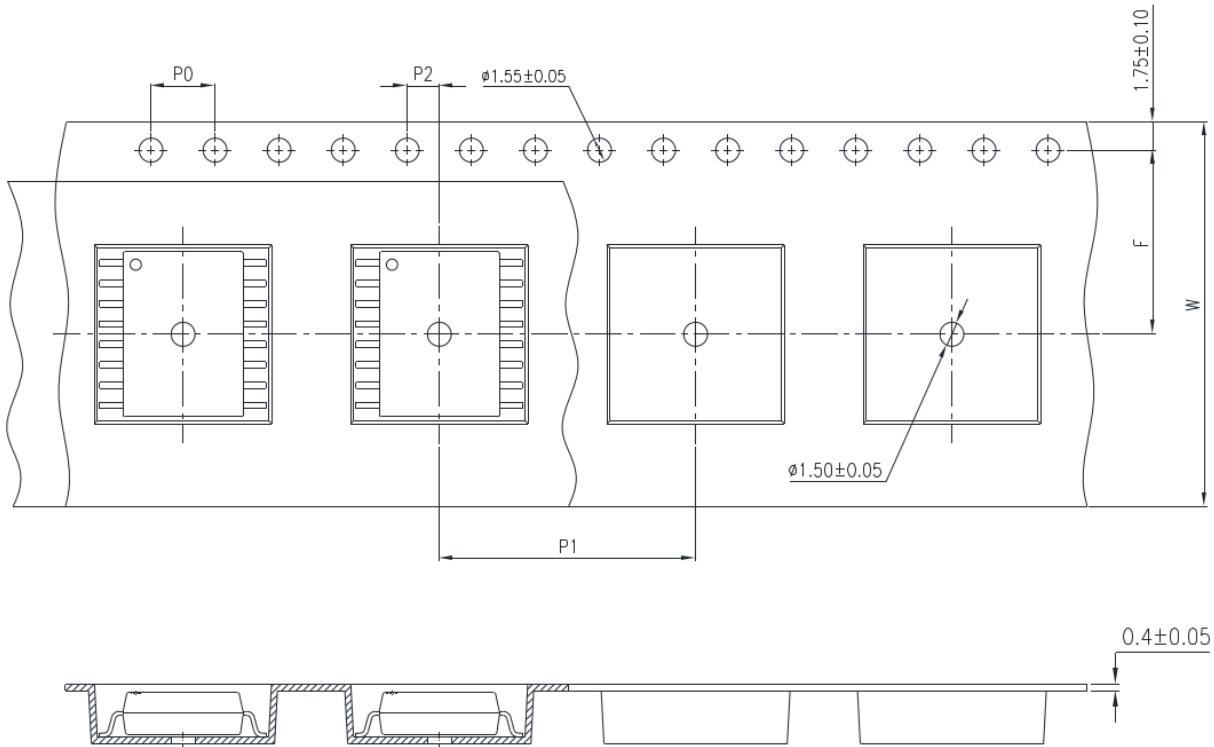




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TAPE AND REEL PACKAGING



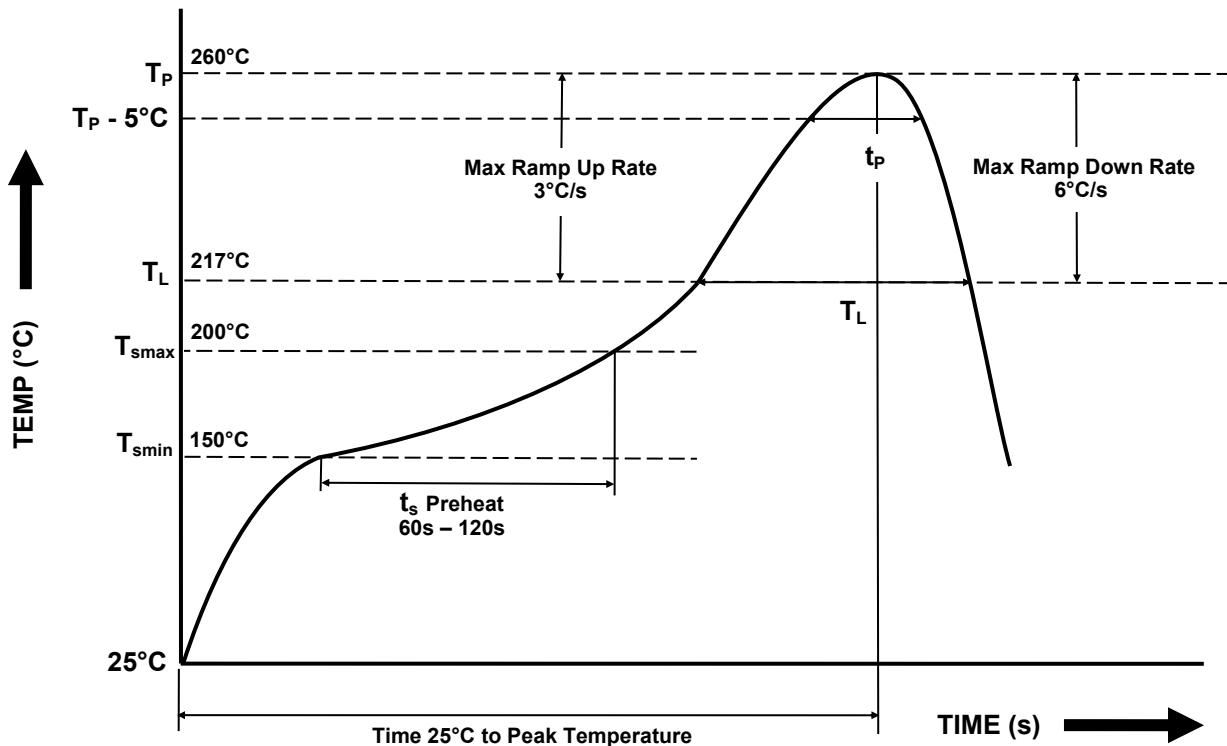
Description	Symbol	Dimension mm (inch)
Tape Width	W	24 ± 0.3 (0.94)
Pitch of Sprocket Holes	P_0	4 ± 0.1 (0.15)
Distance of Compartment to Sprocket Holes	F	11.5 ± 0.1 (0.452)
	P_2	2 ± 0.1 (0.079)
Distance of Compartment to Compartment	P_1	16 ± 0.1 (0.63)



ICPL332J

IR REFLOW SOLDERING TEMPERATURE PROFILE

Note : One Time Reflow Soldering is Recommended.
Do Not Immerse Device Body in Solder Paste.



Profile Details	Conditions
Preheat <ul style="list-style-type: none">- Min Temperature (T_{smin})- Max Temperature (T_{smax})- Time T_{smin} to T_{smax} (t_s)	150°C 200°C 60s - 120s
Soldering Zone <ul style="list-style-type: none">- Peak Temperature (T_P)- Time at Peak Temperature- Liquidous Temperature (T_L)- Time within 5°C of Actual Peak Temperature ($T_P - 5^\circ\text{C}$)- Time maintained above T_L (t_L)- Ramp Up Rate (T_L to T_P)- Ramp Down Rate (T_P to T_L)	260°C 10s max 217°C 30s max 60s - 100s 3°C/s max 6°C/s max
Average Ramp Up Rate (T_{smax} to T_P)	3°C/s max
Time 25°C to Peak Temperature	8 minutes max

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